UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,374	02/02/2000	Masami Kidono	OOCL-11 (11P024627)	6123

26479 7590 12/03/2003

STRAUB & POKOTYLO
620 TINTON AVENUE
BLDG. B, 2ND FLOOR
TINTON FALLS, NJ 07724

EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	17

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/496,374	Applicant(s) KIDONO ET AL.	
	Examiner Jeff Piziali	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on 8 September 2003 (Paper No. 15). These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-9 and 12-23 are rejected under 35 U.S.C. 102(a) as being anticipated by the current application's own admitted prior art.

Regarding claim 1, the background of the current invention discloses a solid-state imaging device comprising: a pixel unit [Fig. 7, 1] constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit [Fig. 7, 2] for vertically transferring charge from the pixels in the pixel unit; a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit; shift gates [Fig. 7, 3] each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes [Fig. 7, 4A] for controlling the shift gates; and a plurality of lead lines [Fig. 7, 4B] and a plurality of connection terminals [Fig. 7, 6] for connecting the gate electrodes to an

external circuit; the gate electrodes making up N [where N = 18, for instance] of gate electrode groups in which the lines belonging to each coset of modulo 18 within successive pixel rows are connected to common lead lines, 18 being a predetermined natural number between 4 and one half the number of pixels [where the number of pixels = 36, for instance] in a column, and also being the minimum number corresponding to the periodic unit about connections from the gate electrodes to the connection terminals within the successive pixel rows, the gate electrodes having common connection terminals to reduce the number (i.e. 16) of the connection terminals to less than 18 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 2, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses gate electrodes/gate control lines [Fig. 7, 4A] connected to gate electrode groups in which horizontal lines belonging to each coset of modulo 18 [where N=18, for instance] within successive pixel rows are connected commonly, being combined with each other so as to reduce the number (i.e. 16) of the connection terminals to less than 18 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 3, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the gate electrodes being provided in a predetermined number 18 [where N = 18, for instance] of gate electrode groups such that the horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo 18, 18 being a predetermined natural number between 4 and one half the number of pixels [where the

number of pixels = 36, for instance] in a column, and also being the minimum number corresponding to the periodic unit about connections from the gate electrodes to the connection terminals within the successive pixel rows, some of the gate electrode groups being commonly connected so that the connection electrodes are less in number (i.e. 16) than 18 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 4, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving (see Fig. 7; Page 4, Line 8 - Page 5, Line 6).

Regarding claim 5, this claim is rejected under the reasoning applied in the above rejection of claims 1, 2 and 4.

Regarding claim 6, this claim is rejected under the reasoning applied in the above rejection of claims 1, 3 and 4.

Regarding claims 7-9, the background of the current invention discloses gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external

circuit (see Fig. 7; Page 4, Line 8 - Page 5, Line 6; where 16 connection terminals is the minimum in this instance).

Regarding claims 12-17, the background of the current invention discloses at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal (see Fig. 7; Page 2, Line 15 - Page 5, Line 6).

Regarding claims 18-23, the background of the current invention discloses only two connection terminals connected to the vertical transfer unit are not connected to any of the gate electrodes (see Fig. 7; Page 2, Line 15 - Page 5, Line 6).

Response to Arguments

4. Applicants' arguments filed 8 September 2003 have been fully considered but they are not persuasive. The applicants contend that the current application's own admitted prior art does not teach some of the gate electrode groups commonly connected so that the connection terminals are less than N, which is a number between 4 and one half the number of pixels in a column and which is also the minimum number of the periodic unit about connections from the gate electrodes to the connection terminals within successive pixel rows. The examiner respectfully disagrees. The prior art embodiment illustrated in Figure 7 shows a repeating pattern of sixteen pixels (labeled as "1-16"). Each pixel #1 is commonly connected to every other pixel #1 -- as well as commonly connected to connection terminal #1 (see Fig. 7; 6). Additionally, each pixel #2 is commonly connected every other pixel #2, and to connection

terminal #2. And so on, for every pixel in the device. However, numbering the pixels as "1-16" is merely a labeling convention. In the instance where the device has thirty-six pixels in a column, instead of labeling the pixels as "1-16, 1-16, 1-4", one skilled in the art would just as easily label the pixels "1-18, 1-18." In either case, there would only exist sixteen connection terminals for thirty-six pixels. In the latter labeling case, pixel #1 and pixel #17 of the first group (of eighteen) would be commonly connected to pixel #15 of the second group -- with all three pixels being commonly connected to connection terminal #1. Furthermore, pixel #2 and pixel #18 of the first group (of eighteen) would be commonly connected to pixel #16 of the second group -- with all three pixels being commonly connected to connection terminal #2.

As such, the current application's own admitted prior art discloses gate electrodes making up N [i.e. 18] of gate electrode groups in which the lines belonging to each coset of modulo 18 within successive pixel rows are connected to common lead lines, 18 being a predetermined natural number between 4 and one half the number of pixels [i.e. 36] in a column, and also being the minimum number corresponding to the periodic unit about connections from the gate electrodes to the connection terminals within the successive pixel rows, the gate electrodes having common connection terminals to reduce the number (i.e. 16) of the connection terminals to less than 18 (see Page 2, Line 15 - Page 5, Line 6). By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
19 November 2003

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600